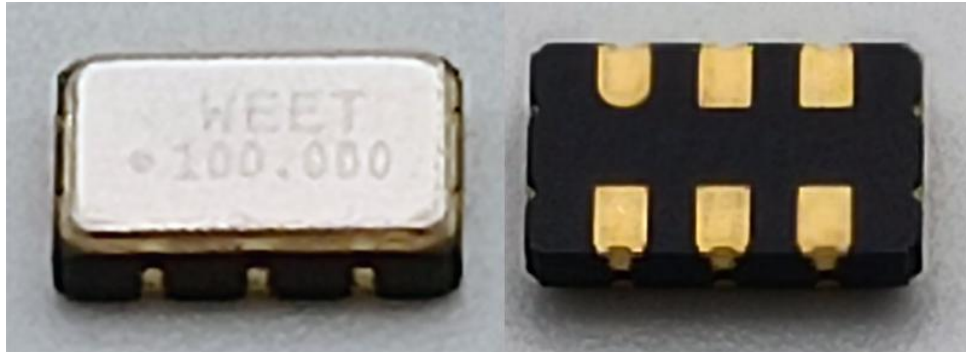


## Features

- Output Types: LVPECL/LVDS/HCSL
- Tri-state function available
- Low Phase Jitter :0.5pSec max.
- Pb-free/RoHS Compliant

## Applications

- Networking and communications
- Gigabit Ethernet
- Fiber Channel
- SONET/SDH



## Frequency Stability & Operating Temperature Range

Temp.	FT	±20ppm	±25ppm	±30ppm	±50ppm
-20°C to +70°C		△	★	★	★
-40°C to +85°C			△	★	★

★: Available    △: Conditional

All condition: Include 25°C tolerance, operating temperature range , input voltage change, aging, load change.

## Electrical Specifications

Item	Symb.	Min.	Typ.	Max.	Unit	Notes
Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000 ,106.250 ,125.000 148.500 ,150.000 ,155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		LVPECL				
Operating Temperature	T <sub>use</sub>	-20		+70	°C	
		-40		+85	°C	
Storage Temperature Range	T <sub>stg</sub>	-55		+125	°C	
Supply Voltage	V <sub>dd</sub>	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L <sub>PECL</sub>		50		Ω	V <sub>dd</sub> - 2.0 V
Current Consumption	I <sub>cc</sub>			50	mA	90MHz ≤ Freq. < 125MHz
				75		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle	SYM	45		55	%	
Rise / Fall Time	T <sub>R</sub> / T <sub>F</sub>			1	nS	20% V <sub>dd</sub> to 80% Level
Start-up Time	T <sub>str</sub>			10	mS	To 90% of Final Amplitude
High output voltage	V <sub>oH</sub>	V <sub>dd</sub> -1.025			V	
Low output voltage	V <sub>oL</sub>			V <sub>dd</sub> -1.62	V	
Enable Voltage High (Logic 1)	V <sub>IH</sub>	0.7V <sub>dd</sub>			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	V <sub>IL</sub>			0.3V <sub>dd</sub>	V	
RMS Phase Jitter	T <sub>RPJ</sub>			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz		-90		dBc/Hz	
	1 KHz		-120		dBc/Hz	
	10 KHz		-140		dBc/Hz	
Aging	f <sub>age</sub>			3	ppm	1st. Year at 25°C



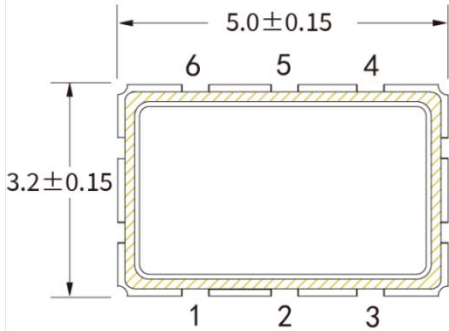
Item	Symb.	Min.	Typ.	Max.	Unit	Notes
Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000,106.250,125.000 148.500,150.000,155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		LVDS				
Operating Temperature	T <sub>use</sub>	-20		+70	°C	
		-40		+85	°C	
Storage Temperature Range	T <sub>stg</sub>	-55		+125	°C	
Supply Voltage	V <sub>dd</sub>	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L <sub>LVDS</sub>		100		Ω	
Current Consumption	I <sub>cc</sub>			30	mA	90MHz ≤ Freq. < 125MHz
				40		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle	SYM	45		55	%	
Rise / Fall Time	T <sub>R</sub> / T <sub>F</sub>			1	nS	20% V <sub>dd</sub> to 80% Level
Start-up Time	T <sub>str</sub>			10	mS	To 90% of Final Amplitude
High output voltage	V <sub>OH</sub>			1.6	V	
Low output voltage	V <sub>OL</sub>	0.9			V	
Enable Voltage High (Logic 1)	V <sub>IH</sub>	0.7V <sub>dd</sub>			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	V <sub>IL</sub>			0.3V <sub>dd</sub>	V	
RMS Phase Jitter	TRPJ			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz		-90		dBc/Hz	
	1 KHz		-120		dBc/Hz	
	10 KHz		-140		dBc/Hz	
Aging	f <sub>age</sub>			3	ppm	1st. Year at 25°C

Item	Symb.	Min.	Typ.	Max.	Unit	Notes
Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000,106.250,125.000 148.500,150.000,155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		HCSL				
Operating Temperature	T <sub>use</sub>	-20		+70	°C	
		-40		+85	°C	
Storage Temperature Range	T <sub>stg</sub>	-55		+125	°C	
Supply Voltage	V <sub>dd</sub>	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L <sub>HCSL</sub>		R <sub>s</sub> =33, R <sub>i</sub> =50		Ω	
Current Consumption	I <sub>cc</sub>			35	mA	90MHz ≤ Freq. < 125MHz
				40		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle		45		55	%	
Rise / Fall Time	T <sub>R</sub> / T <sub>F</sub>			1	nS	20% V <sub>dd</sub> to 80% Level
Start-up Time	T <sub>str</sub>			10	mS	To 90% of Final Amplitude
High output voltage	V <sub>OH</sub>	0.66			V	
Low output voltage	V <sub>OL</sub>			0.15	V	
Enable Voltage High (Logic 1)	V <sub>IH</sub>	0.7V <sub>dd</sub>			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	V <sub>IL</sub>			0.3V <sub>dd</sub>	V	
RMS Phase Jitter	TRPJ			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz		-90		dBc/Hz	
	1 KHz		-120		dBc/Hz	
	10 KHz		-140		dBc/Hz	
Aging	f <sub>age</sub>			3	ppm	1st. Year at 25°C



**Dimensions (mm)**

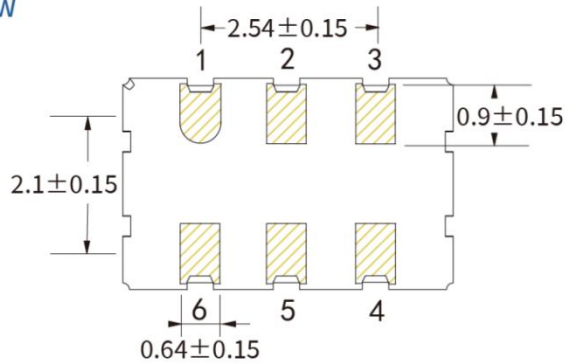
• TOP VIEW



• SIDE VIEW



• BOTTOM VIEW

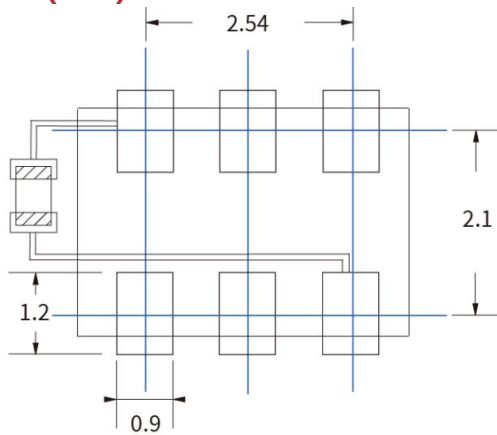


• SIDE VIEW



Pin	Function
1	Tri-State
2	NC
3	GND
4	Output
5	Comp.Output
6	Vdd

**Solder pad layout(mm)**



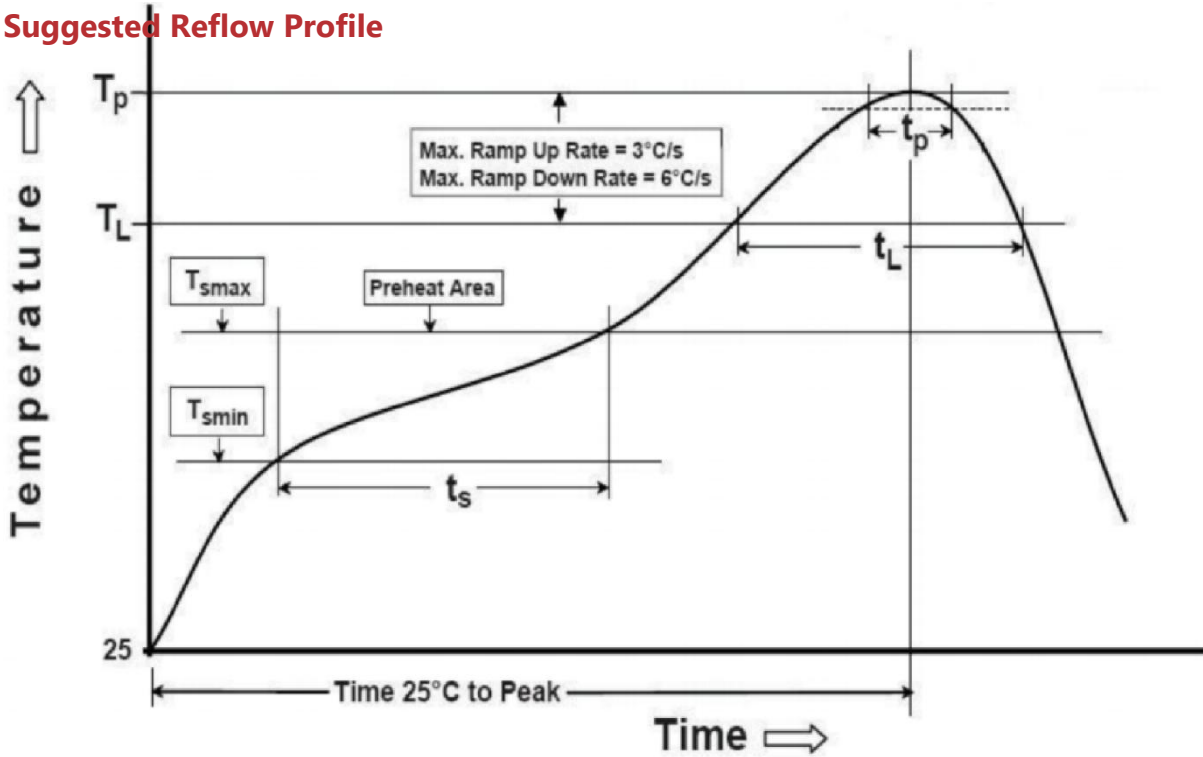
To ensure optimal oscillator performance, place a by-pass capacitor of 0.1µF as close to the part as possible between Vdd and GND pads.

**Product Structure**

- Metal Lid
- Conductive Adhesive, Coated Electrode, Quartz Blank
- IC, Solder Pads, Ceramic Base



**Suggested Reflow Profile**

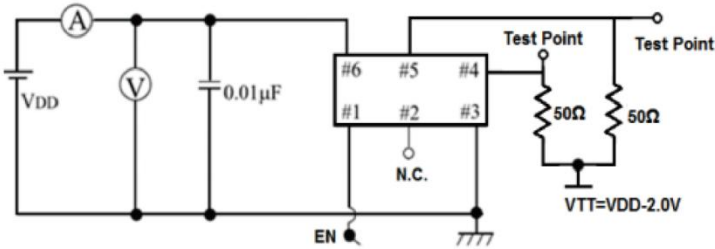


Profile Feature	Sn - Pb Eutectic Assembly	Preheat / Soak
Preheat / Soak ● Temperature Min ( Ts min ) ● Temperature Max ( Ts max ) ● Time ( Ts min to Ts max )	100°C 150°C 60-120 seconds	150°C 200°C 60-120 seconds
Ramp - up rate ( TL to Tp )	3°C/ second max.	3°C/ second max.
Time maintained above ● Liquidous temperature ( TL ) ● Time ( tL ) maintained above TL	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body temperature ( Tp )	235°C	260°C
Time within 5° C of the specified classification temperature ( Tp )	20 seconds	30 seconds
Ramp - down rate ( Tp to TL )	6°C/ second max.	6°C/ second max.
Time 25° C to peak temperature	6 minutes max.	8 minutes max.
<b>Suggest reflow times</b>	<b>2 Times max.</b>	



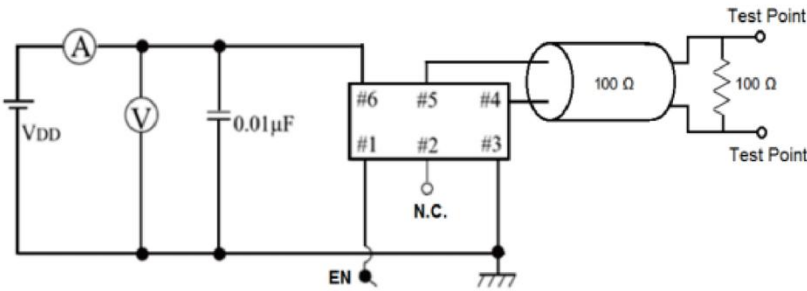
### Testing circuit

- LVPECL



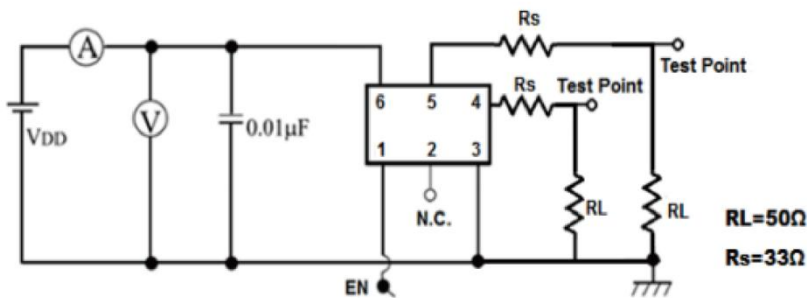
※ Notes: PIN 1 connected to Vdd or floating, the product is working properly; connected to GND, stops working.

- LVDS



※ Notes: PIN 1 connected to Vdd or floating, the product is working properly; connected to GND, stops working.

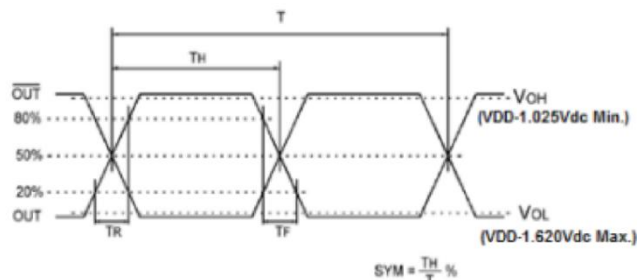
- HCSL



※ Notes: PIN 1 connected to Vdd or floating, the product is working properly; connected to GND, stops working.

### Waveform Conditions

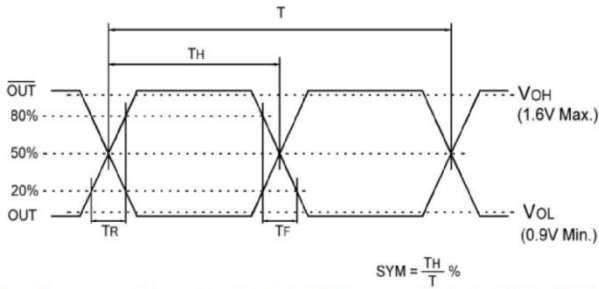
- LVPECL



Waveform measurement system should have a min. bandwidth of 5 times the frequency being tested.

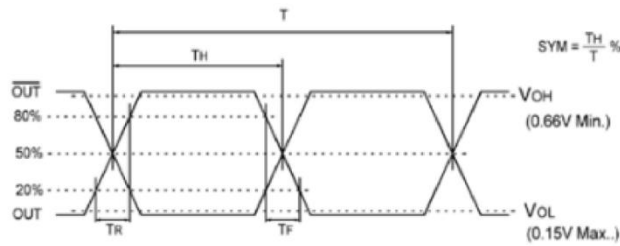


• LVDS



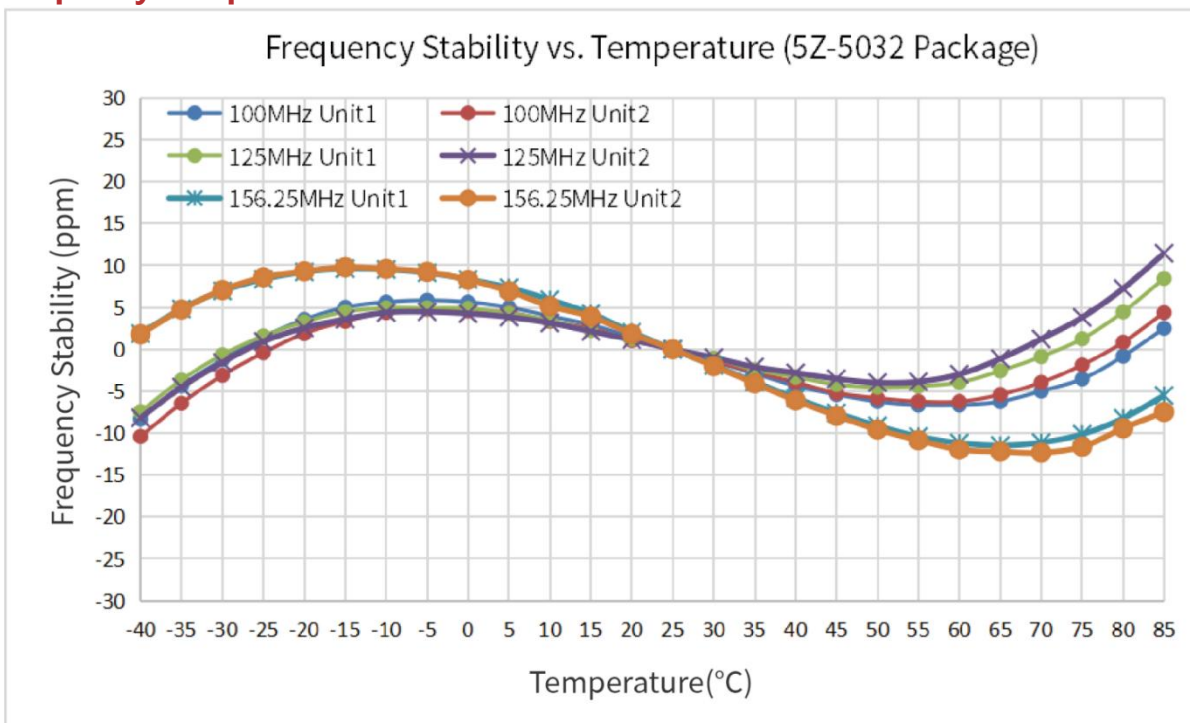
Waveform measurement system should have a min. bandwidth of 5 times the frequency being tested.

• HCSL



Waveform measurement system should have a min. bandwidth of 5 times the frequency being tested.

**Frequency Temperature Characteristics**



**PN Structure:**

WQS-5Z5032100.000B20F30DNNTR

WQS-5Z5032 100.000MHz 3.3V ±20ppm -40+85C ±30ppm LVDS Tape Reel RoHS

WQS-	5Z5032	100.000	B	20	F	30	D	N	N	T	R
Series	Frequency Code(MHz)	Supply Voltage	Frequency Tolerance	Operating Temperature	Frequency Drift	Output	Current Consumption	Phase Noise	Tape Reel	RoHS	
	1	2	3	4	5	6	7	8	9	10	

**1. Frequency Code(MHz)**

100.000	106.250	125.000	148.500	150.000
155.520	156.250			

**2. Supply Voltage**

D	1.8V
H	2.5V
B	3.3V

**3. Frequency Tolerance**

10	±10ppm
20	±20ppm

**4. Operating Temperature**

E	-20+70C
F	-40+85C

**5. Frequency Drift**

15	±15ppm
20	±20ppm
30	±30ppm

**6. Output**

P	LVPECL
D	LVDS
H	HCSL

**7. Current Consumption**

N	Standard
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**8. Phase Noise**

N	Standard
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**9. Packing**

T	Tape Reel
B	Bulk

**10. RoHS**

R	RoHS
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